

Fig. 1

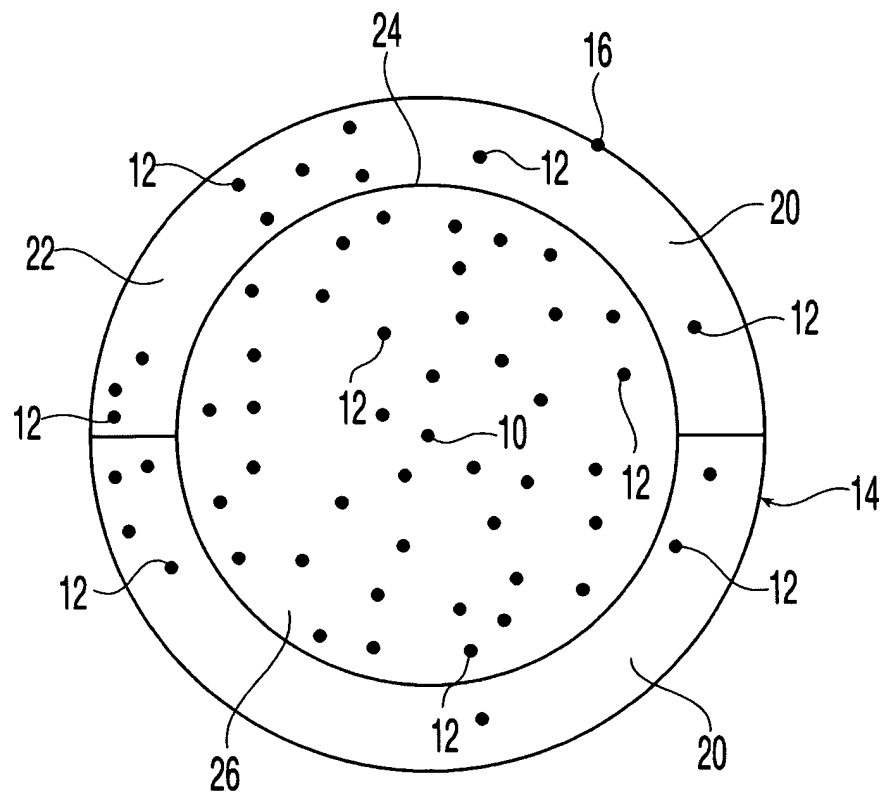


Fig. 2

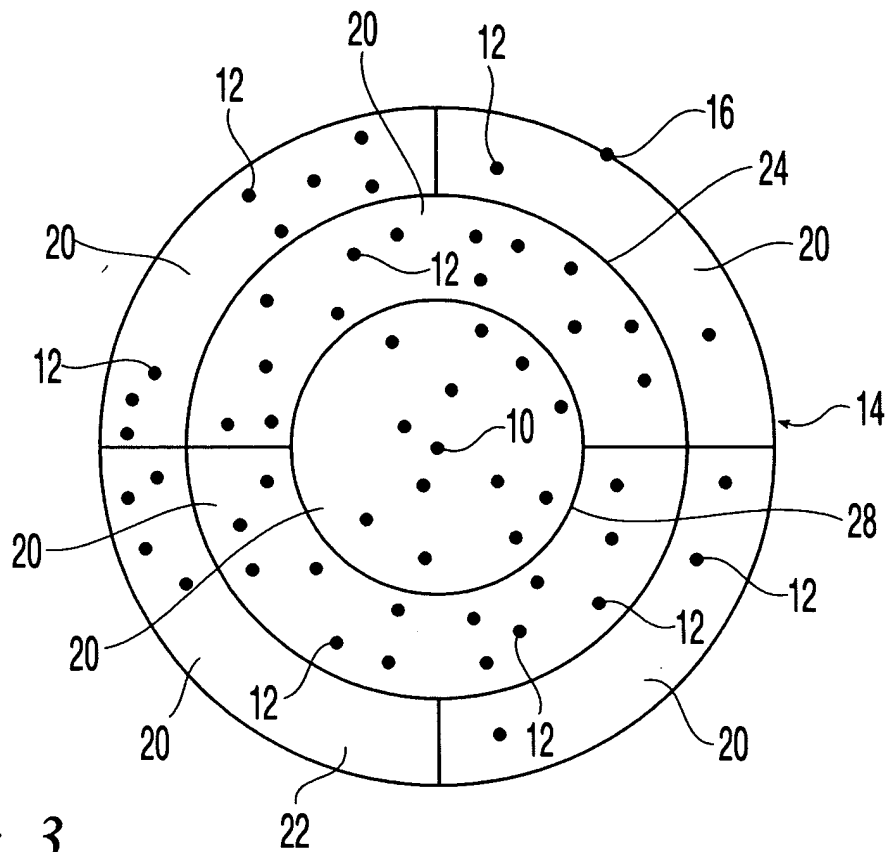


Fig. 3

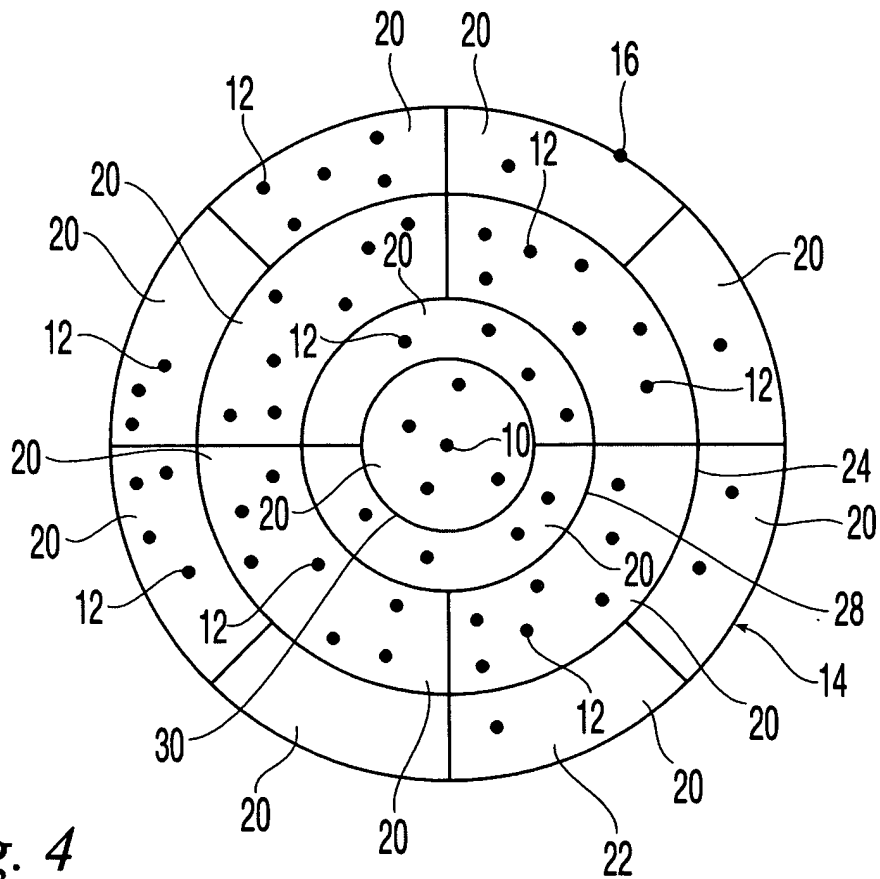


Fig. 4

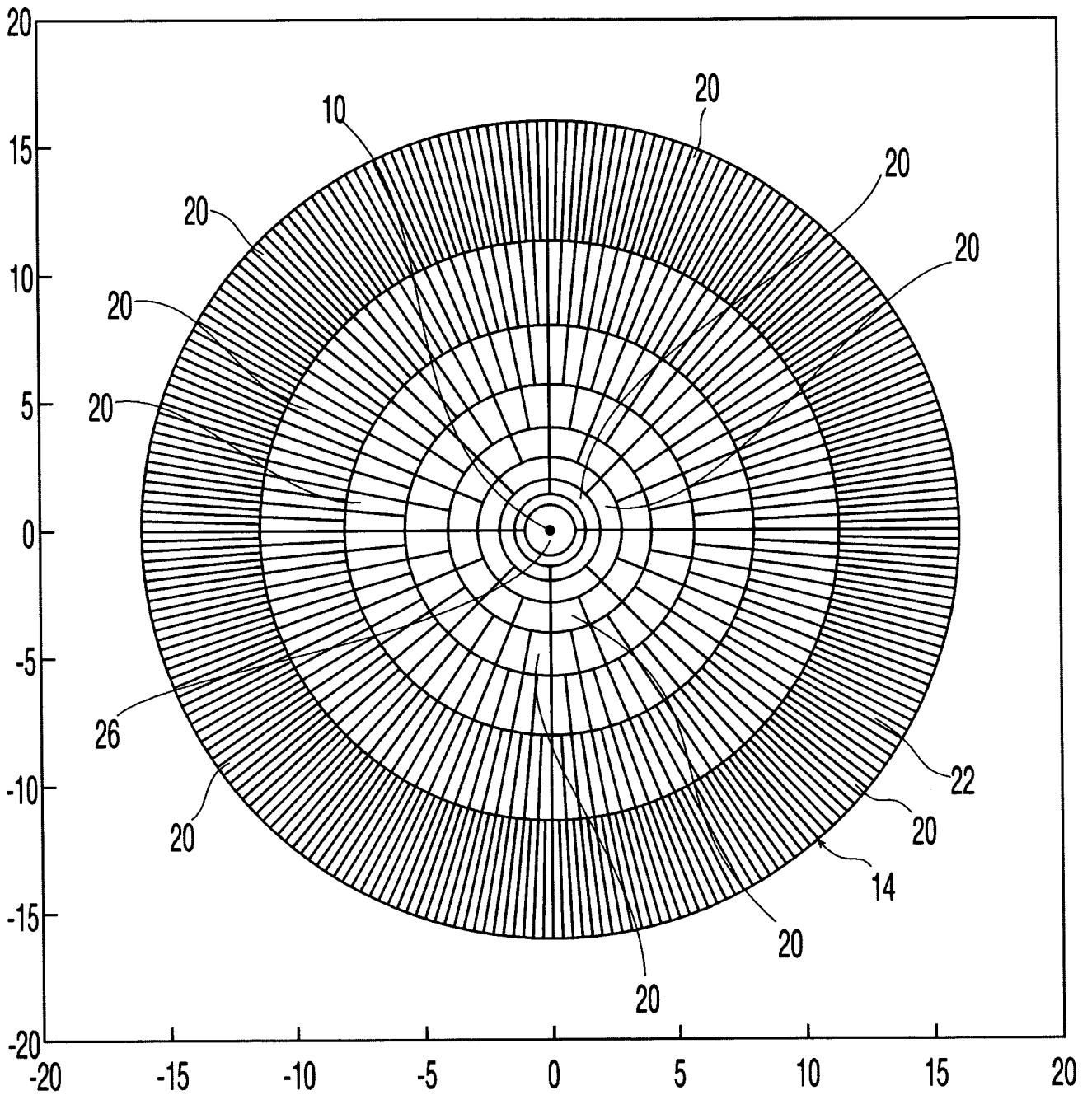


Fig. 5

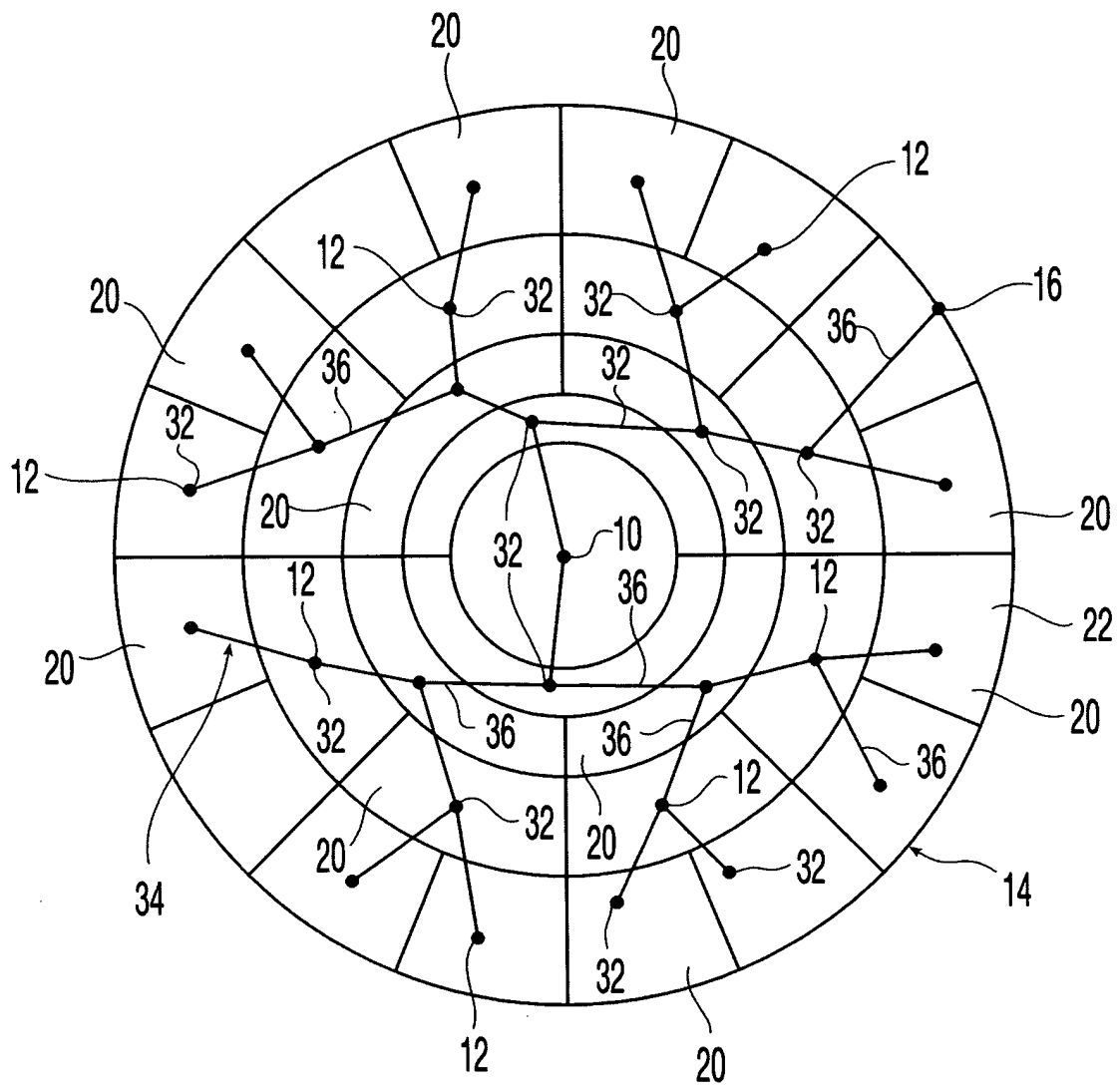


Fig. 6

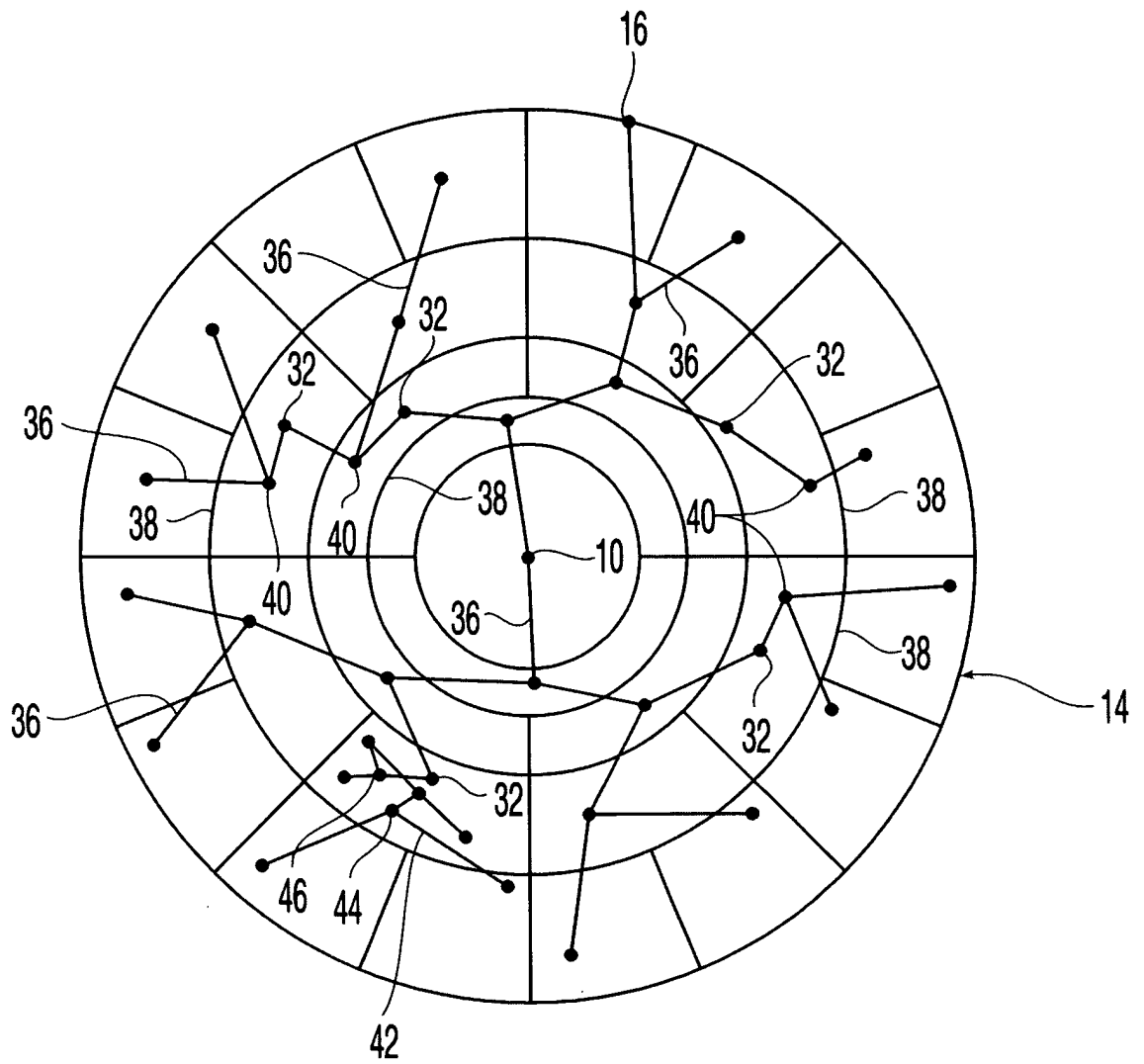


Fig. 7

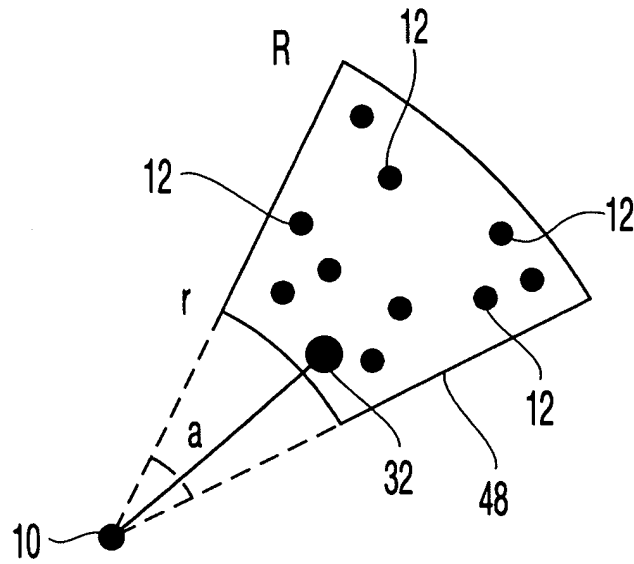


Fig. 8

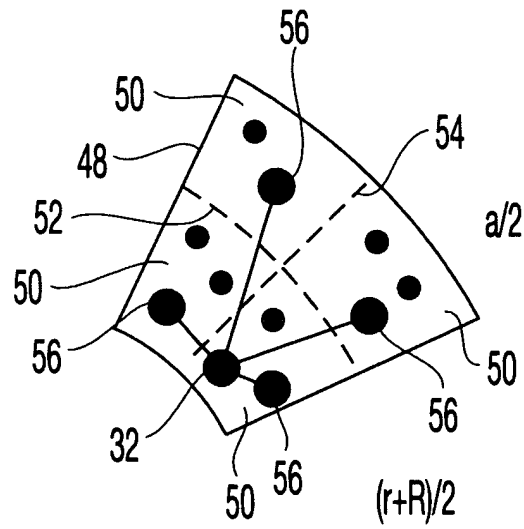


Fig. 9

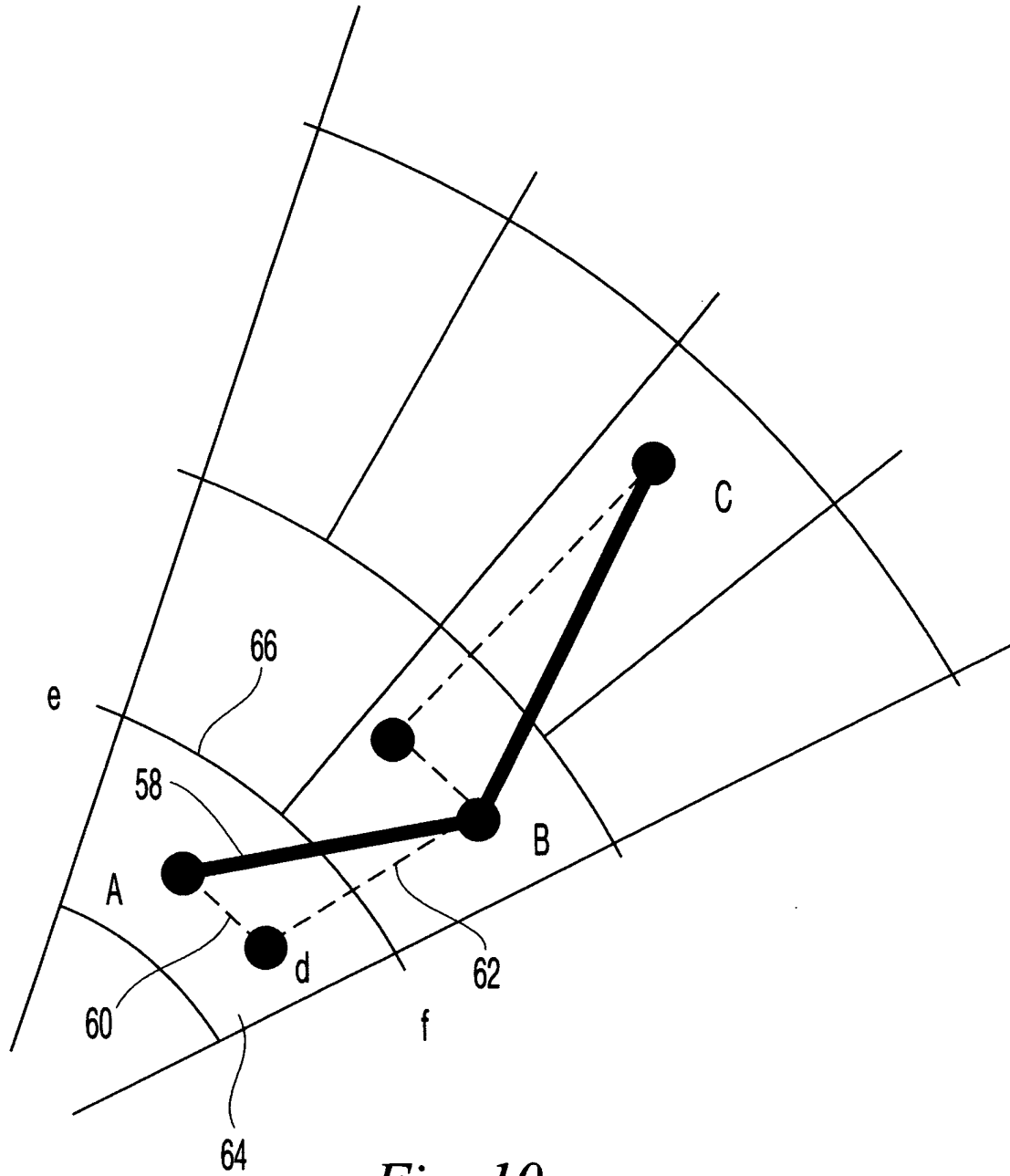


Fig. 10

70	72	74	78	76	80	68					
Out-Degree 6		Out-Degree 2									
Nodes	Rings	Core	Delay	Dev	Bound	CPU Sec	Core	Delay	Dev	Bound	CPU Sec
100	3.61	1.53	1.852	0.20	7.18	0.002	2.21	2.634	0.31	10.74	0.0015
500	5.26	1.22	1.420	0.08	4.92	0.01	1.61	1.876	0.15	6.96	0.01
1,000	6.06	1.13	1.302	0.05	4.09	0.02	1.40	1.622	0.11	5.66	0.02
5,000	8.01	1.00	1.142	0.02	2.65	0.08	1.12	1.285	0.04	3.44	0.08
10,000	8.97	0.99	1.102	0.02	2.20	0.17	1.06	1.202	0.03	2.76	0.17
50,000	11.00	0.94	1.049	0.01	1.61	0.96	0.98	1.095	0.01	1.88	1.02
100,000	11.98	0.95	1.034	0.00	1.43	2.01	0.97	1.067	0.01	1.63	2.13
500,000	14.00	0.92	1.016	0.00	1.22	11.06	0.93	1.031	0.00	1.32	11.84
1,000,000	15.00	0.93	1.012	0.00	1.15	22.99	0.94	1.022	0.00	1.22	24.52
5,000,000	17.00	0.91	1.005	0.00	1.08	132.34	0.91	1.009	0.00	1.11	142.08
		82	86	90	84	88	92				

Fig. 11

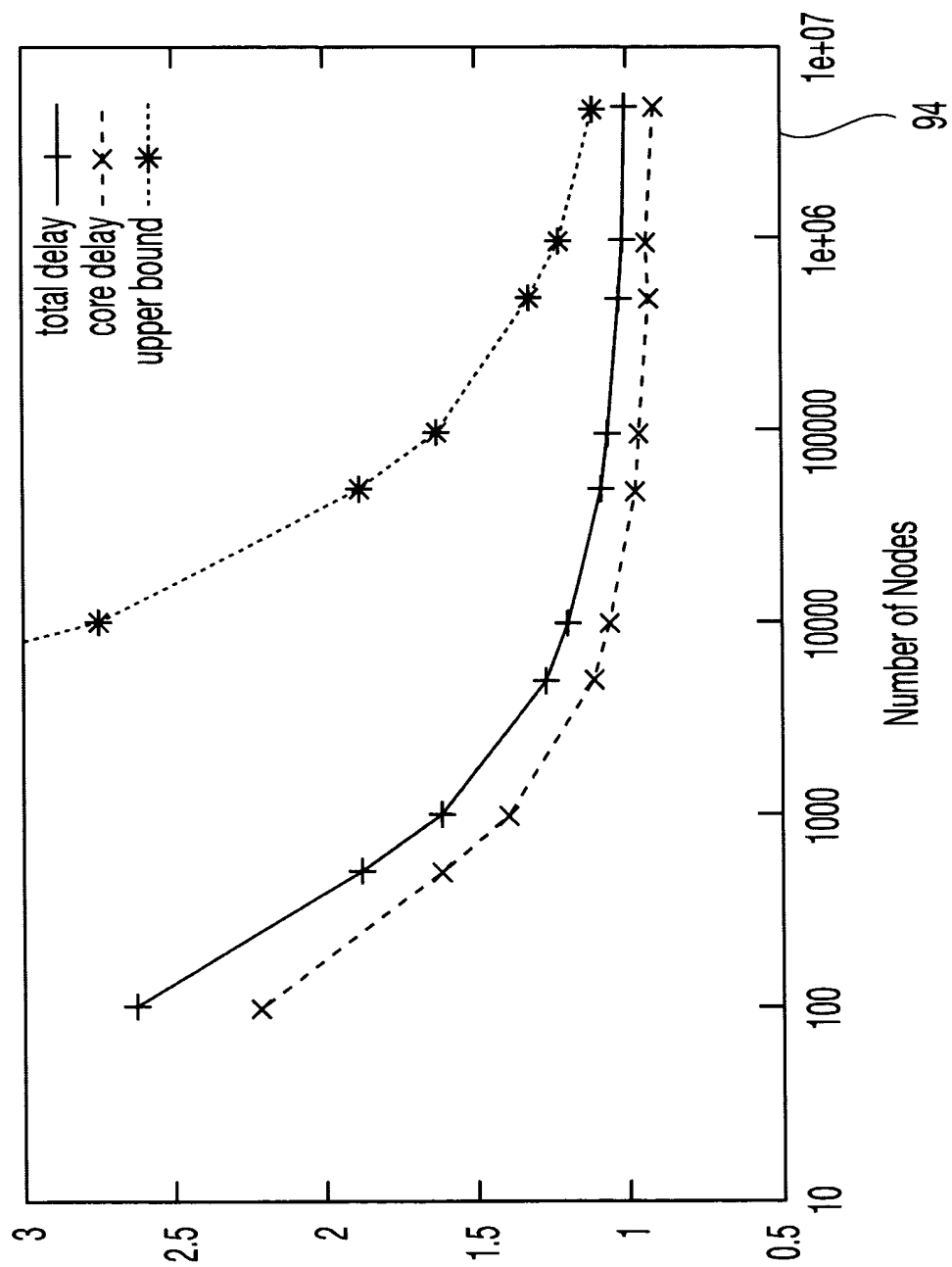


Fig. 12

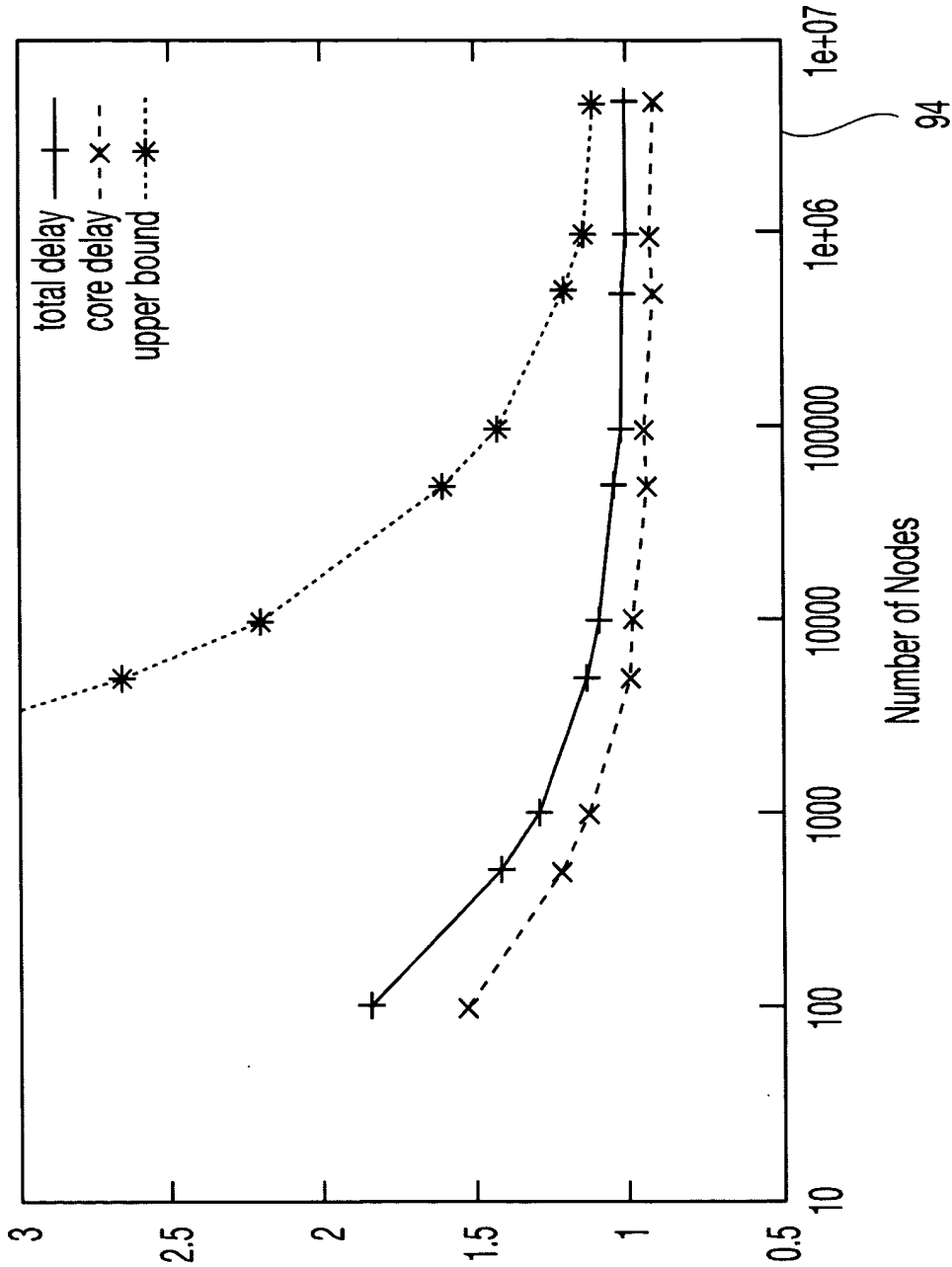


Fig. 13

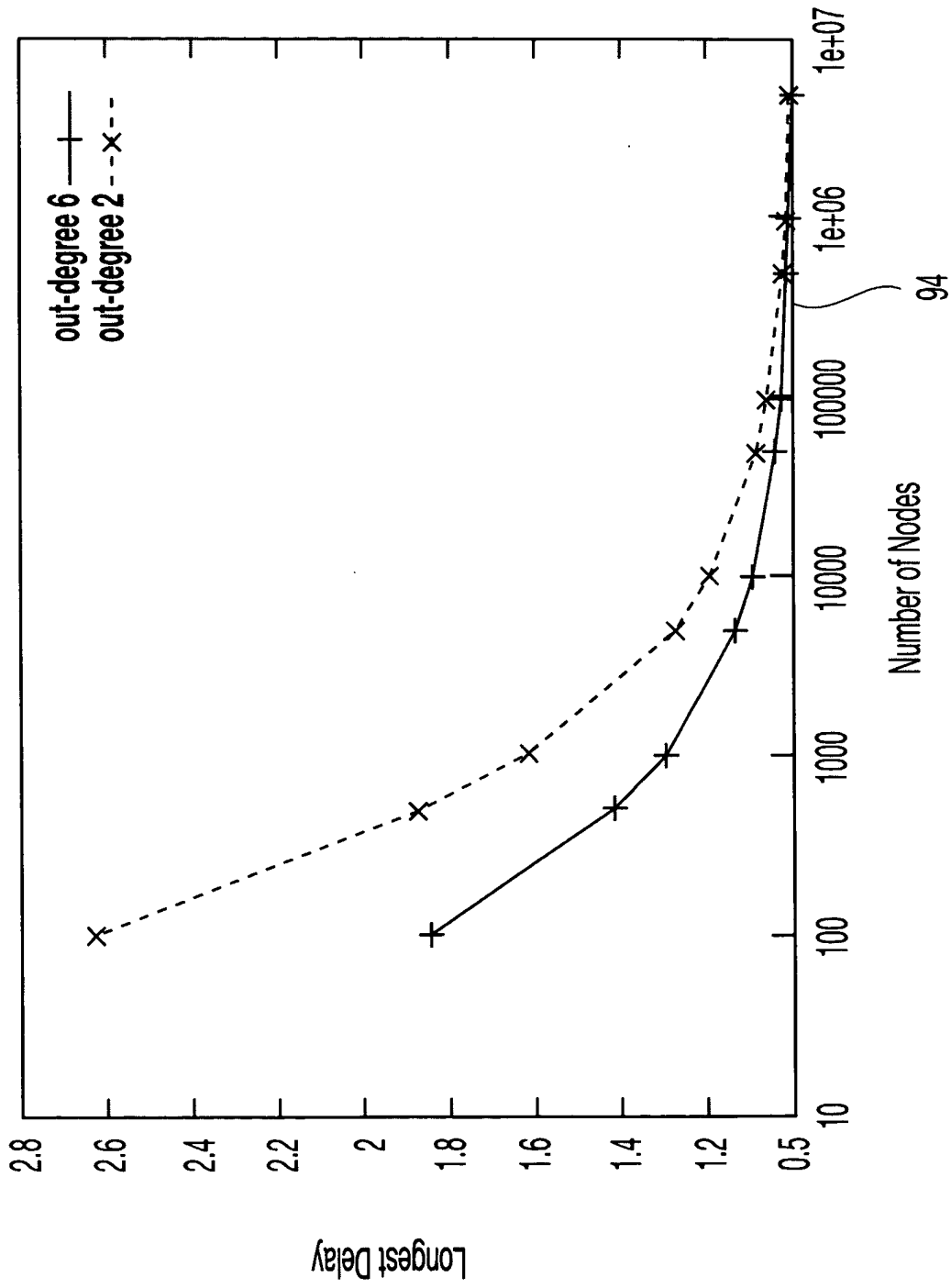


Fig. 14

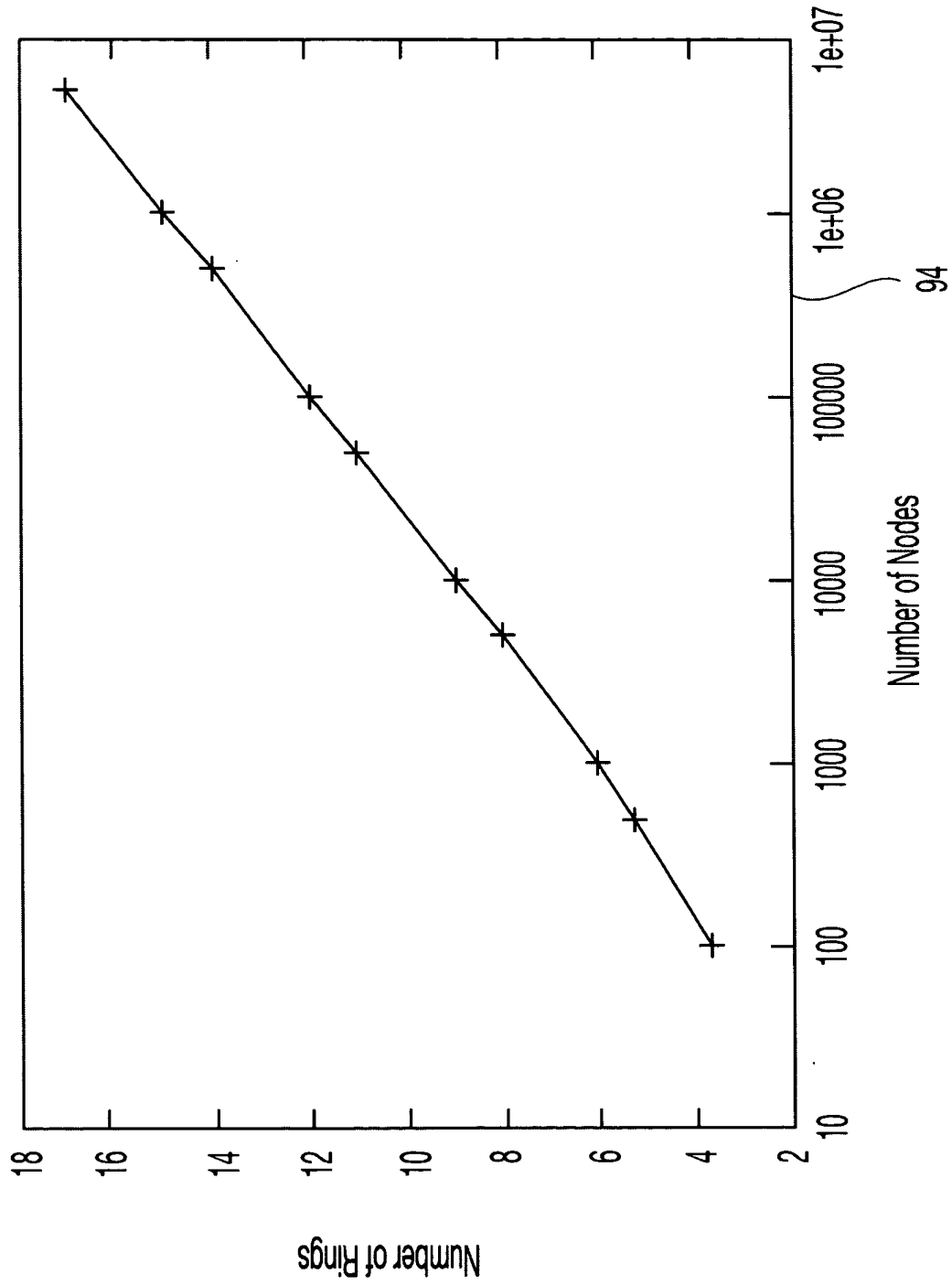


Fig. 15

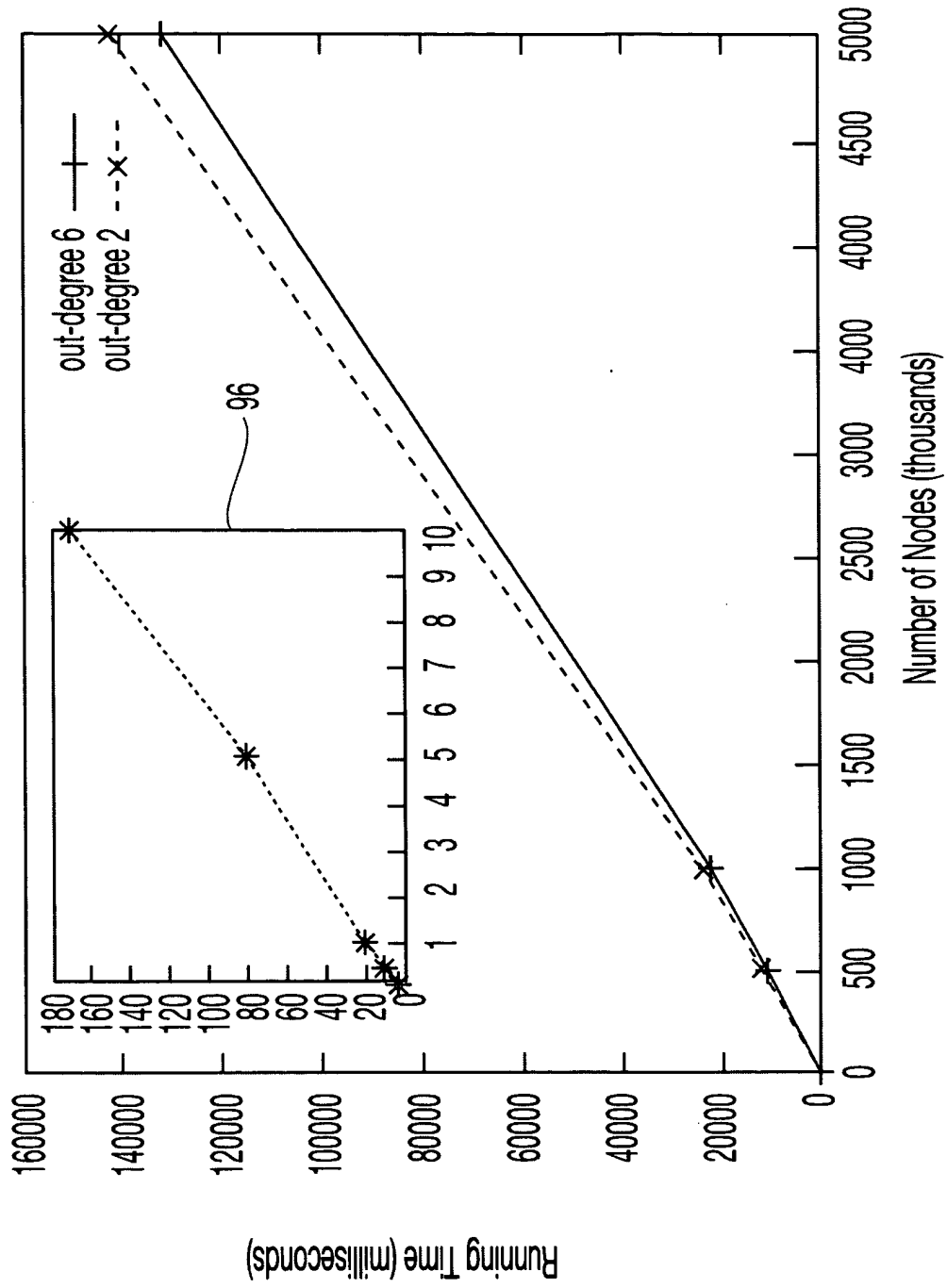


Fig. 16

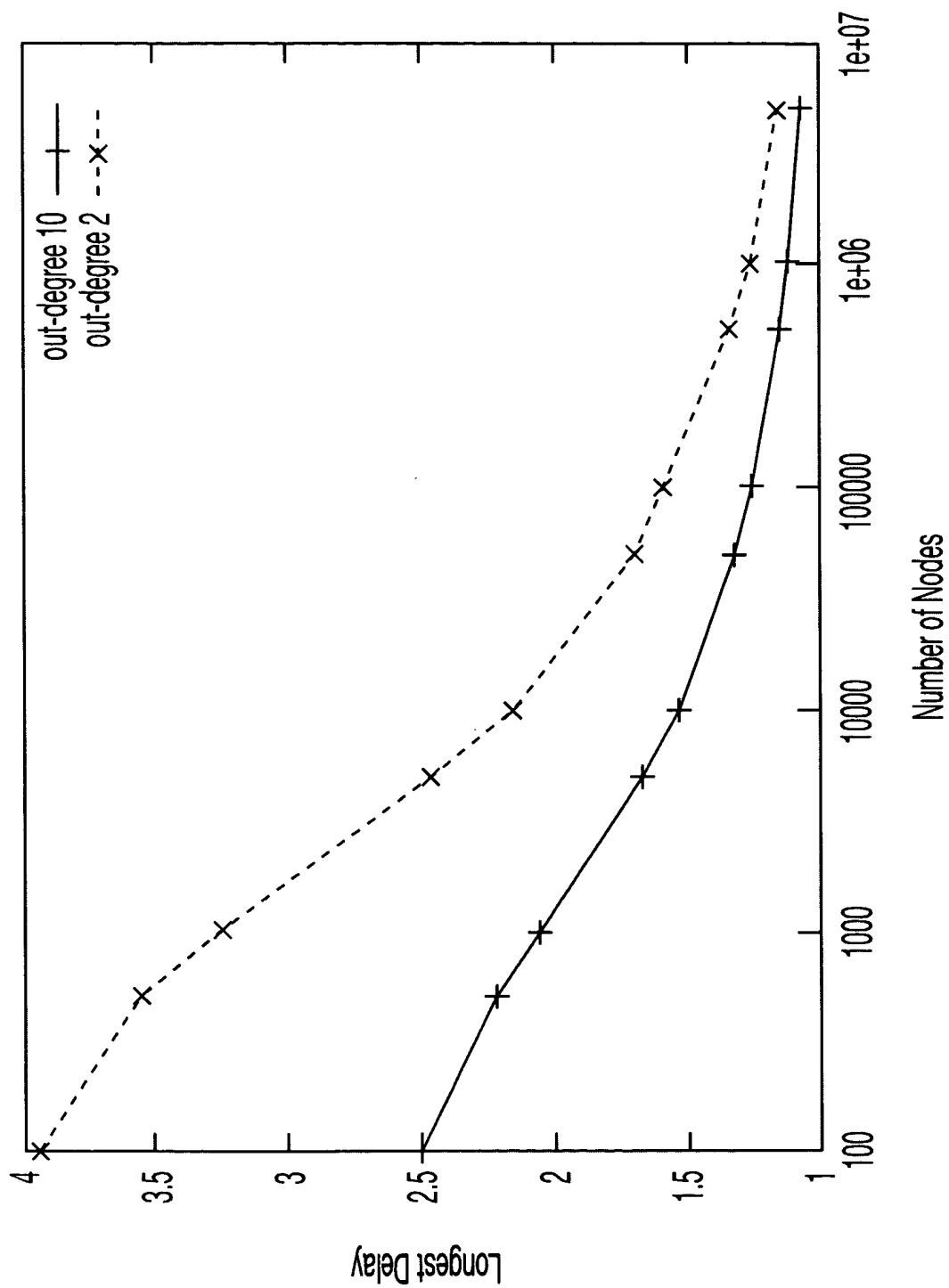


Fig. 17